METHODS FOR QADRATURE MODULATOR IMBALANCE COMPENSATION

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Abstract

Quadrature modulator (demodulator) is used in transmitting (receiving) part of many devices. Modulator (demodulator) output signal can be influenced by unwanted amplitude, phase or DC offset imbalances. MATLAB simulations of imbalances compensation methods and the implementations of simulated methods on the programmable logic filed is a main subject of the paper. Implementations were done with the Xilinx ISE environment. Development kit V2MB1000 with analogue board Memec P160 was chosen for this purpose. Practical measurements and results have been done with digital oscilloscope and digital signal analyzer. Simulation results were compared with practical measurements.

1 Basics of the qadrature modulation and modulator imbalance

IQ imbalance problem arises when non-ideal components injure the power balance or phase orthogonality between inphase (I) and quadrature (Q) branch of modulator. Methods for IQ imbalance compensation are suitable for VHDL implementation in programable logic field. Figure 1 shows block diagram of real modulator with imbalances.

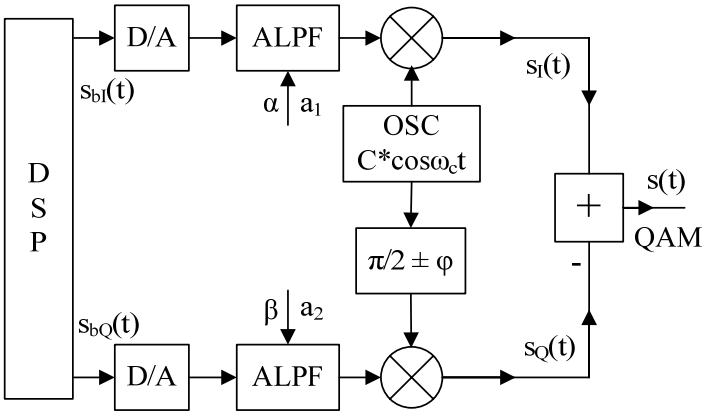

Figure 1: Modulator with imbalances

All of used methods from are based on similar scheme and matrix model. In-phase (I) and quadrature (Q) signals are usually produced in DSP block (digital signal processor). Digital signals are converted into analogue form by digital/analogue converters. Active Low Pass Filter (ALPF) can add unwanted amplitude imbalance (α,β) or DC offset (a_1, a_2). Phase imbalance (φ) express phase difference between both branches, which is figured by the oscillator block and the phase shift block. Adder is the last block of quadrature amplitude modulator. Block diagram and model of quadrature modulator can be described by matrix equation

$$\begin{bmatrix} s_I(t) \\ s_Q(t) \end{bmatrix} = \begin{bmatrix} \alpha\cos(\varphi/2) & \beta\sin(\varphi/2) \\ \alpha\sin(\varphi/2) & \beta\cos(\varphi/2) \end{bmatrix} \cdot \left(\begin{bmatrix} s_{bI}(t) \\ s_{bQ}(t) \end{bmatrix} + \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \right). \quad (1)$$

Where s_{bI} and s_{bQ} denote components of unimpaired signals and other parameters were described before.

2 Methods for imbalance compensation

Compensation of unwanted imbalances of quadrature modulator were published in many articles. Three of them were chosen and simulated.

2.1 Method by Cavers [1]

Mathematic describtion of modulator with imbalances is shown in the matrix equation (1). The compensation method is based on inverse matrix compensating of imbalances. Algorithm uses iteration steps to find the coefficients. Convergence or divergence of the algorithm depends on the iteration step size. Only signal envelope has to be known to find the compensation coefficients. Four signals were used as training sequences with same amplitude and different phase. The compensation was finished when four different input signals resulted in same output signals. New compensation matrix coefficients are given by:

$$\begin{aligned} c_{12}(k+1) &= c_{12}(k) - \delta \cdot f_p\left(e_g(k), e_p(k)\right) \\ c_{22}(k+1) &= c_{22}(k) - \delta \cdot f_g\left(e_g(k), e_p(k)\right) \end{aligned}. \tag{2}$$

Where new coefficients ($c_{12}(k+1)$, $c_{22}(k+1)$) are computed from previous coefficients $c_{12}(k)$ and $c_{22}(k)$. Parameter δ represents size of iteration step and $f_p\left(e_g(k), e_p(k)\right)$ describes matching error.

2.2 Method by Zhu [4]

Modulator was described with similar matrix equation (1). Method was ideal for signals with constant envelope. Algorithm is trying to find compensation matrixes ***P(n)*** and ***d(n)***. Constant modulus algorithm adjusting the ***P(n)*** and ***d(n)*** to minimize the cost function *J(n)*, which provides a measure of the amplitude fluctuation. Is defined as

$$J(n) = E\left[\left(\left\| \tilde{\mathbf{s}}(n) \right\|^2 - R_2\right)^2\right] \tag{2}$$

Where E is the mathematical expectation operator and R_2 is a constant depending only on the input data symbol $\tilde{\mathbf{s}}(n)$. Variable R_2 is defined as

$$R_2 = \frac{E\left[\left\|\mathbf{s}_m(n)\right\|^4\right]}{E\left[\left\|\mathbf{s}_m(n)\right\|^2\right]}. \tag{3}$$

The compensation coefficients ***P(n)*** and ***d(n)*** can be adapted by using stochastic gradient algorithm. The adaptation consists of adjusting ***p(n)*** with a step size μ in the opposite direction of estimated gradient and is given by

$$\mathbf{p}(n+1) = \mathbf{p}(n) - \mu \cdot e(n)\mathbf{x}_t(n). \tag{4}$$

Where $e(n) = \left\| \tilde{\mathbf{s}}(n) \right\|^2 - R_2$, vector ***p(n)*** denotes compensation coefficients ***P(n)*** and ***d(n)***: $\left[p_{11}(n) \quad p_{12}(n) \quad p_{21}(n) \quad p_{22}(n) \quad d_I(n) \quad d_Q(n)\right]^T$ and vector $\mathbf{x}_t(n)$ represents:

$$\mathbf{x}_t(n) = \left[\tilde{I}_m^2(n) \quad \tilde{I}_m(n)\tilde{Q}_m(n) \quad \tilde{Q}_m(n)\tilde{I}_m(n) \quad \tilde{Q}_m^2(n) \quad \tilde{I}_m(n) \quad \tilde{Q}_m(n)\right]^T \tag{5}$$

The value of step size is a tradeoff between the speed of convergence and estimated jitter in the steady state.

2.3 Method by Held [2]

Method was published by Ingolf Held in paper [2]. IQ imbalance can be characterized by two parameters: amplitude imbalance K_I, K_Q as a power mismatch between I and Q branch, and phase imbalance φ_{err} as an error of orthogonality between I and Q branch. Situation can be characterized by the matrix equation:

$$\begin{bmatrix} s_I[k] \\ s_Q[k] \end{bmatrix} = \begin{bmatrix} K_I & 0 \\ -K_Q \cdot \sin\varphi_{err} & K_Q \cdot \cos\varphi_{err} \end{bmatrix} \cdot \begin{bmatrix} s_I'[k] \\ s_Q'[k] \end{bmatrix}. \tag{6}$$

Where s'_I and s'_Q denote components of unimpaired signals. Estimate of amplitude imbalance is based on the following equation:

$$K_{est} = \sqrt{\frac{\sum_{k=1}^{L} \left| s_Q^2[k] \right|}{\sum_{k=1}^{L} \left| s_I^2[k] \right|}}. \tag{7}$$

The long-time domain preamble has been used as a training input sequence s consisting of s_I and s_Q parts. Parameter L denotes a number of long preamble samples to compute the estimation. Estimation of phase imbalance coefficient P_{est} uses the same data symbols s of length L. The following equation is used

$$P_{est} = \frac{\sum_{k=1}^{L} \left(s_I[k] \cdot s_Q[k] \right)}{\sum_{k=1}^{L} s_I^2[k]}. \tag{8}$$

When both of compensation coefficients are found, correction of imbalances can continued. Estimate from (7) is used to asymmetrically correct amplitude imbalance and estimate from (8) is used to correct phase imbalance. Situation is described by:

$$\begin{aligned} w_I[k] &= \frac{1}{K_{est}} \cdot s_I[k] \\ w_Q[k] &= \frac{1}{\sqrt{1 - P_{est}^2}} \left[s_Q[k] - P_{est} \cdot s_I[k] \right] \end{aligned}. \tag{9}$$

Variables w_I, w_Q denote output corrected (compensated) signals.

3 MATLAB simulations

MATLAB was chosen as an ideal simulation environment. Results can be displayed as a constellation diagrams or any others charts. Usually constellation diagrams give the basic information about modulator states and imbalances. For example Figure 2 displays imbalances of the modulator before and after compensation. Results are displayed for method proposed by Held [2].

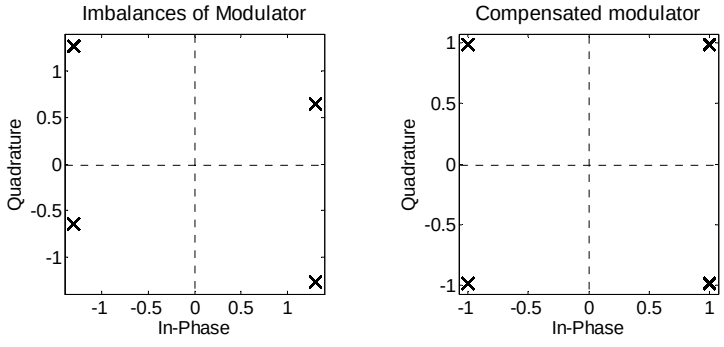

Figure 2: Constellation diagrams showing the Imbalances of Modulator (left) and Compensated Modulator (right)

Parameters were set as follows amplitude imbalances $\alpha = 1,3$ and $\beta = 1$, phase imbalance $\varphi = \pi /10rad$. It's evident that both of imbalances have been compensated. Quality of compensations depends on the settings of methods. All of simulated methods have advantages and disadvantages.

Example of the iteration step (δ) influence on the algorithm convergence Figure 3. Charts correspond to method proposed by Cavers [1]. Graph shows mean square error and number of iterations for different setting of parameter δ.

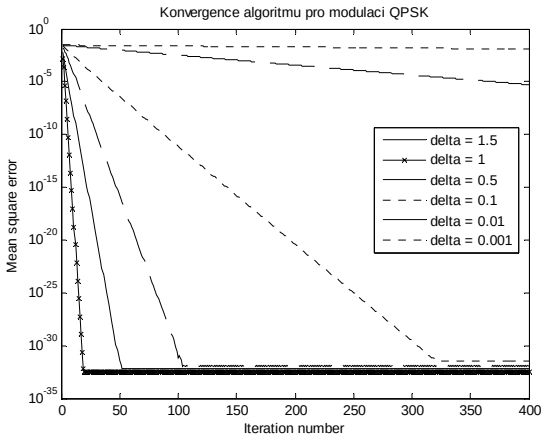

Figure 3: Convergence of algorithm [1] with QPSK modulation

Iteration step size was chosen as compromise between speed of convergence and number of iterations. Smaller iteration step δ corresponds to need more iterations. Ideal step size was chosen $\delta = 1$.

4 Xilinx implementation of method by Held [2]

After succesfull MATLAB simulations, the Xilinx ISE environment was used for implementation. The compensation algorithm had to be rebuilt for VHDL implementation. The basic blocks are shown on simplified schematic (Figure 4).

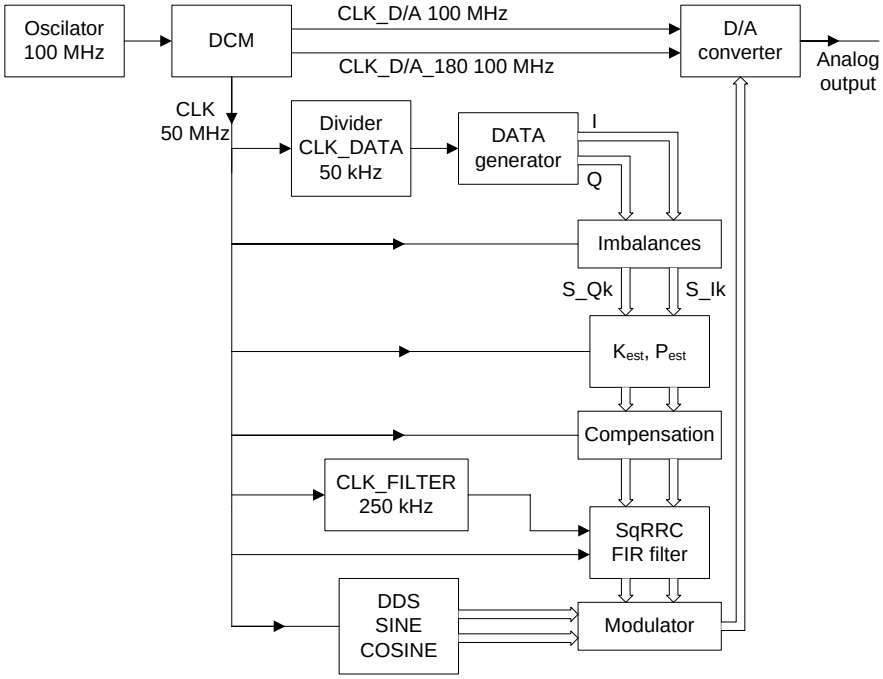

Figure 4: Block diagram of implemented method by Held [2]

Clock speed of FPGA was 100 MHz. Digital Clock Manager (DCM) provided clocking for other blocks. Random symbols (s'_I and s'_Q) were generated by DATA generator. Data symbols passed through the model of imbalances. Next steps were calculating compensation coefficients, imbalance compensation, filtering signals by Square Root Raised Cosine filter (elimination inter symbol interferences) and modulation on the carrier with frequency 500 kHz. All of mathematic operations were done in floating point format. The development kit V2MB1000 has been used for the

implementation. Almost 100% logic blocks inside FPGA were used. Signal from modulator has been sent into analogue board Memec P160 with the D/A converter. Output analogue signal could be measured and displayed by digital oscilloscope and digital signal analyzer.

5 Output measurements of implemented method

The output analogue signal was measured in the time domain. Oscilloscope screen is displayed on Figure 5. Measurement results corresponded with simulations in ModelSim and also with Matlab.

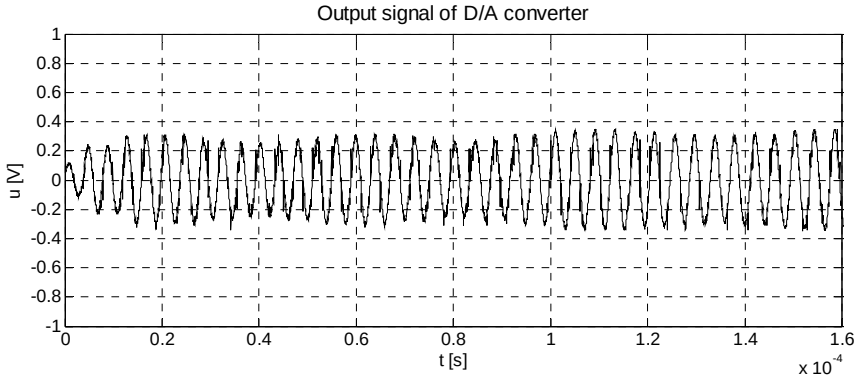

Figure 5: Output analogue signal after D/A conversion

Digital signal analyzer (Rohde & Schwarz FSQ3) was used for display constellation diagrams of signal before compensation (with amplitude imbalances $K_I = 1,1$and $K_Q = 0,9$, phase imbalance $\varphi_{err}=\pi /10rad$) and after compensation (without imbalances). The graphic results are shown on Figure 6.

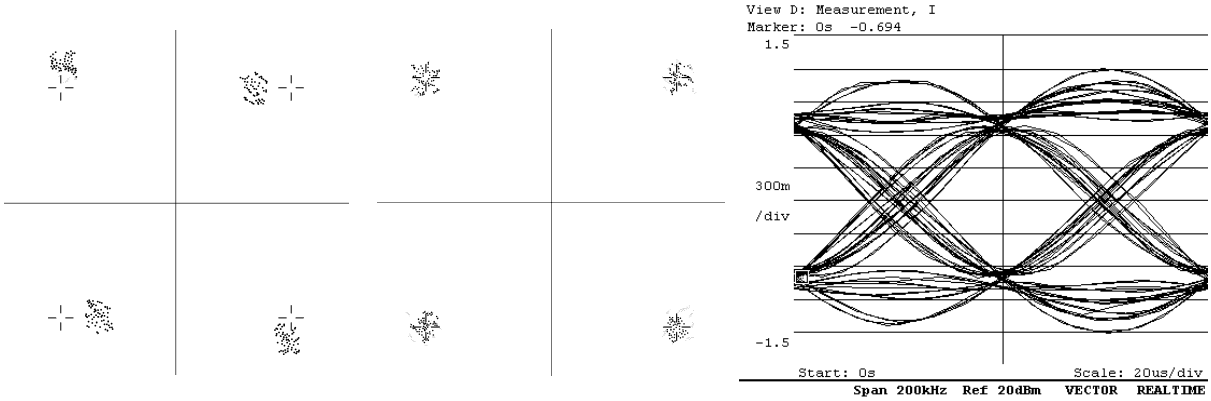

Figure 6: Constellation diagrams before (left) and after compensation (centre). Eye diagram of I branch of modulator (right)

It's evident that both of imbalances have been compensated. The constellation points have been dispersed as a consequence of shorter impulse response of used raised cosine filter. The Eye diagram of I branch of modulator is displayed on Figure 6 (right). Diagram is a confirmation of inter symbol interferences.

6 Conclusion

Three methods were chosen for quadrature modulator imbalance compensation. Each of them was simulated and results were compared in the MATLAB environment. Constellation diagrams show states of modulator and quality of compensation. Simulations also confirm number of iteration steps with different step size.

The VHDL implementation was started with simulation in the ModelSim environment. Results correspond with simulations before. As an ideal FPGA implementation method the one proposed by Held [2] was chosen. Number of logic blocks used in FPGA Virtex II XC2V1000 reached almost 100%. Method was implemented together with data generation, filter for elimination of inter symbol

interferences and direct digital synthesizer that generated a carrier for the modulator. Measured results proved right function of implemented method.

Acknowledgments

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