AD 612 Data Acquisition Card

USER'S MANUAL

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Introduction Introduction

1. Introduction

1.1. General Description

The AD 612 data acquisition card is designed for the need of connecting PC compatible computers to real world signals. The AD 612 contains a 100 kHz throughput 12 bit A/D converter with sample/hold circuit, four software selectable input ranges and 8 channel input multiplexer, 4 independent 12 bit D/A converters, 8 bit digital input port and 8 bit digital output port. The card is designed for standard data acquisition and control applications and optimized for use with Real Time Toolbox for MATLAB®. Because of the small size and low power consumption AD 612 can be used not only in desktop computers but also in portable computers.

1.2. Features List

The AD 612 offers following features:

- 10 μs 12 bit A/D converter with sample & hold circuit
- 8 channel single ended fault protected input multiplexer
- Software selectable input ranges ±10V, ±5V, 0-10V, 0-5V
- Internal voltage reference
- 4 D/A converters with 12 bit resolution and ± 10 V output range
- 8 bit TTL compatible digital input port
- 8 bit TTL compatible digital output port
- Interrupt

- Requires one PCI slot
- Power consumption 300 mA@+5V, 50 mA@+12V, 50 mA@-12V
- Operating temperature 0° C to $+70^{\circ}$ C

1.3. Specifications

1.3.1. A/D Converter

Resolution: 12 bits

Number of channels: 8 single ended

Conversion time: $10 \mu s$

 $\pm 10V$, $\pm 5V$, 0-10V, 0-5V, software selectable Input ranges:

Input protection: $\pm 16.5V$ Input impedance: $> 10 \text{ k}\Omega$

1.3.2. D/A Converter

Resolution: 12 bit 4

Number of channels:

Settling time: max. 10 μs (1/2 LSB)

Slew Rate: $10 \text{ V/}\mu\text{s}$ Output current: min. ±5 mA Short circuit current: ±30 mA DC output impedance: 0.1Ω

Load capacitance: max. 500 pF Differential nonlinearity: ±1 LSB

Gain drift: typ. ±5 ppm/K Zero drift: typ. ±5 ppmFSR/K

1.3.3. Digital Inputs

Number of bits: 8

Input signal levels: TTL

Logic 0: 0.8 V max. Logic 1: 2.0 V min.

1.3.4. Digital Outputs

Number of bits: 8
Output signal levels: TTL

Logic 0: 0.5 V max. @ 24 mA (sink)
Logic 1: 2.0 V min. @ 15 mA (source)

2. Installation

2.1. Board Installation

AD 612 has no switches or jumpers and you can install it in any free PCI expansion slot of your computer. Follow the steps outlined below:

- Turn off the power of the computer system and unplug the power cord.
- Disconnect all cables connected to the computer system.
- Using a screwdriver, remove the cover-mounting screws. These screws are at the rear side of the PC.
- Remove the computer system's cover.
- Find an empty expansion slot in your computer for AD 612 card. If the slot still has the metal expansion-slot cover attached, remove the cover with a screwdriver. Save the screw to install the AD 612.
- Hold the AD 612 firmly at the top of the board, and press the gold edge connector into an empty PCI expansion slot.
- Using a screwdriver, screw the retaining bracket tightly against the rear plate of the computer system.
- Replace the cover of the computer, and plug in the power cord.
- Reconnect all cables that were previously attached to the rear of the computer.

2.2. Driver Installation

Once you have installed AD 612 to PCI slot you can install Windows driver. Follow the steps outlined below:

Turn on the computer, boot Microsoft Windows. AD 612 is detected by system automatically. In Add Hardware Wizzard window click Next.



Insert installation floppy into drive a. In Found New Hardware Wizzard select Install the software automatically and click Next.



When prompted for driver location type a:\ and click Next. Click Finish to complete installation.





3. Programming Guide

3.1. I/O Port Map

AD 612 uses PCI Vendor ID 0x186C and Device ID 0x0612. I/O space of AD 612 card consists of 5 regions:

Region	Function	Size (bytes)
BADR0 (I/O mapped)	Board programming registers	16
BADR1 (I/O mapped)	Reserved	4
BADR2 (I/O mapped)	OX9162 local configuration registers	32
BADR3 (memory mapped)	OX9162 local configuration registers	4096
BADR4 (memory mapped)	Board programming registers	4096

Table 9. Base Address Register Regions

Address	Read	Write
BADR0+0	ADLO - A/D data low	ADCTRL - A/D control
BADR0+1	ADHI - A/D data high	
BADR0+2		
BADR0+3		
BADR0+4		
BADR0+5		
BADR0+6	DIN - Digital input	DOUT - Digital output
BADR0+7		
BADR0+8	DALE - D/A latch enable	DA0LO - D/A 0 data low byte
BADR0+9		DA0HI - D/A 0 data high byte
BADR0+A		DA1LO - D/A 1 data low byte
BADR0+B		DA1HI - D/A 1 data high byte
BADR0+C		DA2LO - D/A 2 data low byte
BADR0+D		DA2HI - D/A 2 data high byte
BADR0+E		DA3LO - D/A 3 data low byte
BADR0+F		DA3HI - D/A 3 data high byte
BADR2+10	STATUS - Status register	

Table 2. I/O Port Map

3.2. A/D Converter

All functions of A/D converter are accessible through four registers.

A/D control register **ADCTRL** is used to select input channel, input range and to start conversion. For ADCTRL bit assignment see table 3.

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
0	1	0	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7		Must be always 0
6		Must be always 1
5		Must be always 0
4	RNG	Selects 10V input range (see table 4)
3	BIP	Selects bipolar input range (see table 4)
2, 1, 0	A2, A1, A0	Selects input channel (see table 5)

Table 3. A/D Control Byte Format

RNG	ВІР	INPUT RANGE (V)
0	0	0 to 5
1	0	0 to 10
0	1	± 5
1	1	± 10

Table 4. Input Range Selection

A2	A1	A0	СНО	CH1	CH2	СНЗ	СН4	СН5	СН6	СН7
0	0	0	*							
0	0	1		*						
0	1	0			*					
0	1	1				*				
1	0	0					*			
1	0	1						*		
1	1	0							*	
1	1	1								*

Table 5. Input Channel Selection

Conversion is initiated with a write operation to **ADCTRL** register (located at address BADR0+0) which also selects the input multiplexer channel and input range. When the conversion is complete bit 2 in status register **STAT** (BARD2+10) is set to zero. Then the data is ready and can be read from **ADLO** and **ADHI** registers (BADR0+0, BADR0+1). The read operation of **ADLO** and **ADHI** registers sets the conversion complete bit in **STAT** register back to one. Writing a new control byte during conversion cycle will abort current conversion and start a new conversion cycle. **CC** can generate system interrupt if **CCINTE** bit in Status register is set.

D20 - D31 (MSB)	D19	D18	D4 - D17	D3	D2	D0 - D1 (LSB)
Res.	T5INTE	CCINTE	Res.	T5	CC	Res.

Table 6. Status Register Format

	D7	D6	D5	D4	D3	D2	D1	D 0
ADLO	D7	D6	D5	D4	D3	D2	D1	D0
ADHI	0 or	0 or	0 or	0 or	D11	D10	D9	D8
	D11	D11	D11	D11				

Table 7. A/D Data Registers Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading **ADLO** the lower eight bits are read. When reading **ADHI** the upper four MSBs are available and the output data bits D4-D7 are either set 0 (in unipolar mode) or set to the value of MSB (in bipolar mode) as described in Table 7.

A/D converter voltage reference can be adjusted by R7.

Sample code for A/D conversion:

unsigned short BADR0, BADR2;

```
int ch;
short ad;
char Gain[8];

// start conversion on channel ch
outp(BADR0, ch | (Gain[ch]<<3) | 0x40);

// wait until conversion completed
while (ISBIT1(inp(BADR2+10),0x04));

// read data
ad=inp(BADR0)+(inp(BADR0+1)<<8);

// convert to bipolar range
ad-= Gain[ch] & 0x1 ? 0 : 0x800;

// convert to double
return(ad/(double) (1<<11));
```

3.3. D/A Converters

D/A converters are accessed through eight data input latch registers (**DA0LO**, **DA0HI**, **DA1LO**, **DA1HI**, **DA2LO**, **DA2HI**, **DA3LO**, **DA3HI**). D/A converters do not require any initialization. All analog outputs are updated simultaneously by read from D/A latch register **DALE** (BAR0+8).

	D7	D6	D5	D4	D3	D2	D1	D 0
DALO	D7	D6	D5	D4	D3	D2	D1	D0
DAHI	0	0	0	0	D11	D10	D9	D8

Table 8. D/A Data Registers Format

Output voltage ranges of D/A converters are $\pm 10V$. After power-on or hardware reset the output voltage is set to 0V.

Digital input	Output Voltage
0xFFF	9.9951 V
0x800	0.0000 V
0x7FF	-0.0049 V
0x000	-10.0000 V

Table 9. D/A Outputs

3.4. Digital I/O

AD 612 contains one 8-bit digital input port and one 8-bit digital output port. Digital input port can be accessed directly by read from **DIN** register (BADR+6). Inputs are TTL compatible. Digital output port can be accessed by write to **DOUT** register (BADR+6). Outputs are TTL compatible. After power-on or hardware reset digital outputs are set to 0.

4. I/O Signals

4.1. Output Connector Signal Description

The AD 612 multifunction I/O card is equipped with an on-board 37 pin D-type female connector X1. For pin assignment refer to Tables 15 and 16. TB 620 Terminal Board can be connected to X1 connector.

AD0-AD7 Analog inputs
DA0-DA3 Analog outputs

DIN0-DIN7 TTL compatible digital inputs

DOUT0-DOUT7 TTL compatible digital outputs
+12V +12V power supply
-12V -12V power supply
+5V +5V power supply
AGND Analog ground
GND Digital ground

450			
AD0	1	20	DA0
AD1	2		DA1
AD2	3	21	
AD3	4	22	AGND
AD4	5	23	DA2
AD5	6	24	DA3
	7	25	AGND
AD6		26	-12V
AD7	8	27	+12V
AGND	9	28	+5V
AGND	10	29	GND
GND	11		
DIN0	12	30	DOUT0
DIN1	13	31	DOUT1
DIN2	14	32	DOUT2
		33	DOUT3
DIN3	15	34	DOUT4
DIN4	16	35	DOUT5
DIN5	17	36	
DIN6	18		DOUT6
DIN7	19	37	DOUT7

Table 15. X1 Connector Pin Assignement

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